IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A functional block for an integrated circuit, ~~characterized by~~ comprising a test data output circuit for outputting test data responsive to a control signal indicating a test data transmission state.

2. (Currently Amended) The functional block for an integrated circuit of Claim 1, characterized in that the test data output circuit includes a plurality of output signal lines enabling parallel output, and

outputs the test data such that an adjacent pair of the output signal lines have mutually different values.

3. (Currently Amended) The functional block for an integrated circuit of Claim 1, characterized in that the test data output circuit outputs the test data changing from one value into the other.

4. (Currently Amended) The functional block for an integrated circuit of Claim 1, characterized in that the test data output circuit includes a plurality of output signal lines enabling parallel output, and

outputs the test data such that an adjacent pair of the output signal lines have mutually different values, and that each of the output signal lines outputs the test data alternately changing from one value into the other and vice versa.

5. (Currently Amended) The functional block for an integrated circuit of Claim 1, characterized in that the test data output circuit includes a plurality of output signal lines enabling parallel output,

divides the output signal lines into a number 2n of groups, where n is an integer equal to or larger than one, and

outputs the test data such that the respective groups divided have mutually different values, which change from one value into the other.

6. (Currently Amended) The functional block for an integrated circuit of Claim 1, characterized in that the test data output circuit includes:

an original data generating section for generating and outputting first and second original data, the first original data being composed of zeros and ones alternately arranged, the second original data being obtained by inverting the first original data; and

a selector circuit for receiving the first and second original data and selecting either the first or second original data in response to a selection signal externally supplied, thereby outputting the test data.

7. (Currently Amended) The functional block for an integrated circuit of Claim 6, characterized in that the test data output circuit includes a plurality of the selector circuits, and

further includes a shift register for receiving the selection signal and outputting the input selection signal to each said selector circuit.

8. (Currently Amended) The functional block for an integrated circuit of Claim 1, characterized in that the test data output circuit includes:

an original data generating section for generating and outputting original data composed of zeros and ones alternately arranged; and

a plurality of inverter circuits, each receiving the original data, and

that control signals with mutually inverted values are input to the inverter circuits, which output the test data with mutually inverted values.

9. (Currently Amended) The functional block for an integrated circuit of Claim 8, characterized in that the test data output circuit further comprises a shift register for receiving the control signal and outputting the input control signal to each said inverter circuit.

10. (Currently Amended) The functional block for an integrated circuit of Claim 1, characterized in that the test data output circuit includes:

a plurality of test data generating sections for generating mutually different test data; and

a test data selecting section for selecting one of the test data generating sections responsive to the control signal.

11. (Currently Amended) The functional block for an integrated circuit of Claim 1, ~~characterized by~~ further comprising a decision result output circuit for receiving the test data responsive to a control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision.

12. (Currently Amended) The functional block for an integrated circuit of Claim 1, ~~characterized by~~ further comprising a testing standby circuit for blocking the output of an output signal responsive to a control signal indicating a testing standby state.

13. (Currently Amended) The functional block for an integrated circuit of Claim 12, characterized in that the test data output circuit includes an inverted data generating section for inverting a value of the test data responsive to the control signal indicating the testing standby state.

14. (Currently Amended) The functional block for an integrated circuit of Claim 1, ~~characterized by~~ further comprising:

a decision result output circuit for receiving the test data responsive to a control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision; and

a testing standby circuit for blocking the output of an output signal responsive to a control signal indicating a testing standby state.

15. (Currently Amended) The functional block for an integrated circuit of Claim 14, characterized in that the test data output circuit includes an inverted data generating section for inverting a value of the test data responsive to the control signal indicating the test data reception state.

16. (Currently Amended) A functional block for an integrated circuit, ~~characterized by~~ comprising a decision result output circuit for receiving test data responsive to a control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision.

17. (Currently Amended) The functional block for an integrated circuit of Claim 16, characterized in that the decision result output circuit includes a plurality of expected value comparing sections, each comparing the test data to an expected value of the test data.

18. (Canceled)

19. (Currently Amended) The functional block for an integrated circuit of Claim 16, characterized in that the decision result output circuit includes holding means for holding the decision result thereon.

20. (Currently Amended) The functional block for an integrated circuit of Claim 19, characterized in that the holding means is a shift register.

21 – 32. (Canceled)